

HIGH PERFORMANCE VERTICAL PNP TRANSISTOR AND METHOD

Abstract of the Disclosure

The invention includes a method and resulting structure for fabricating high performance vertical NPN and PNP transistors for use in BiCMOS devices. The resulting high performance vertical PNP transistor includes an emitter region including silicon and germanium, and has its PNP emitter sharing a single layer of silicon with the NPN transistor's base. The method adds two additional masking steps to conventional fabrication processes for CMOS and bipolar devices, thus representing minor additions to the entire process flow. The resulting structure significantly enhances PNP device performance.

Figures